

March 10, 2010

Track 1		Track 2	
8:30 AM	Registration, Gateway Foyer Breakfast, Fir and Oak Rooms, Second Floor		
9:00 AM	Welcome Address Fir and Oak Rooms, Second Floor		
Session 1	Strategies & Techniques for Reducing Turnaround Time Pine Room	Testing 1, 2, 3: The Latest DFT Techniques Cedar Room	
9:15 AM	65-nm Design Tape-Out in 6 weeks	Adapteva Inc.	AltaSens Inc. and Mentor Graphics
10:00 AM	Multi-Mode/Multi-Corner Analysis Using Talus	Wipro	Magma Talus Design with Scan Test Compression
10:45 AM	Guest Keynote: 3D ICs: New Directions for Semiconductors , Robert Patti, CTO, Tezzaron Semiconductor Siskiyou Room, First Floor		
11:15 AM	CEO Keynote: The Electronic Ocean , Rajeev Madhavan, CEO, Magma Siskiyou Room, First Floor		
11:55 AM	Lunch Panel: Semiconductor Venture Funding – At a Crossroads? Fir and Oak Rooms, Second Floor		
Session 2	Challenges of Full-Flow RTL-to-GDSII SoC Implementation Pine Room	Leveraging Faster, More Accurate Circuit Simulation Cedar Room	
12:40 PM	Comparing Crosstalk Delay Calculations in Talus and Prime Time-SI	Qthink	At-Speed Functional Verification of Complex I/Os using FineSim SPICE
1:25 PM	Leveraging Quartz DRC Capabilities on Advanced Server Processors in 45 nm and Beyond	IBM	Rapid Bridge
2:10 PM	Break		
Session 3	Taming the Dragon: Managing Multi-Scenario Analysis and Timing Closure Pine Room	Advances in Analog Design and IC Failure Analysis Cedar Room	
2:25 PM	Timing Closure Challenges and Solutions	Magma	Using the Titan Shape-Based-Router for Actel's Next-Generation Flash-Based FPGA Product Family
3:10 PM	Accelerating Timing Closure on Large, Complex Nanometer Designs	Server Engines	Actel Inc.
Tutorial Pine Room		Tutorial Cedar Room	
3:55 PM	Solving Design Challenges Visually with the Talus Visual Volcano	Magma	Using SiliconSmart ACE and Embedded FineSim Simulator for 28-nm Standard I/O Cell and Memory Characterization
4:55 PM	Partners Fair and Cocktail Reception Donner Room, First Floor		