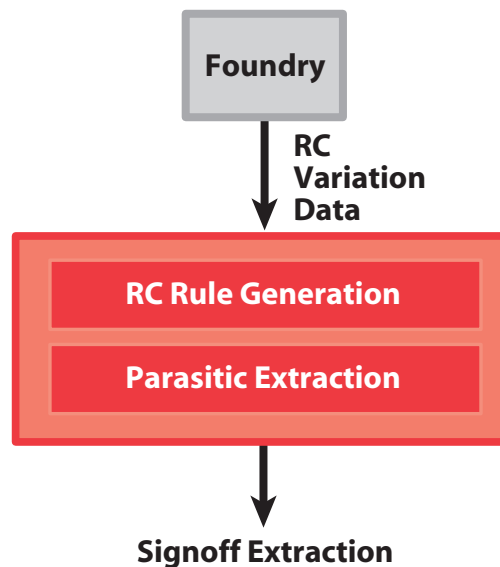


Quartz™ RC

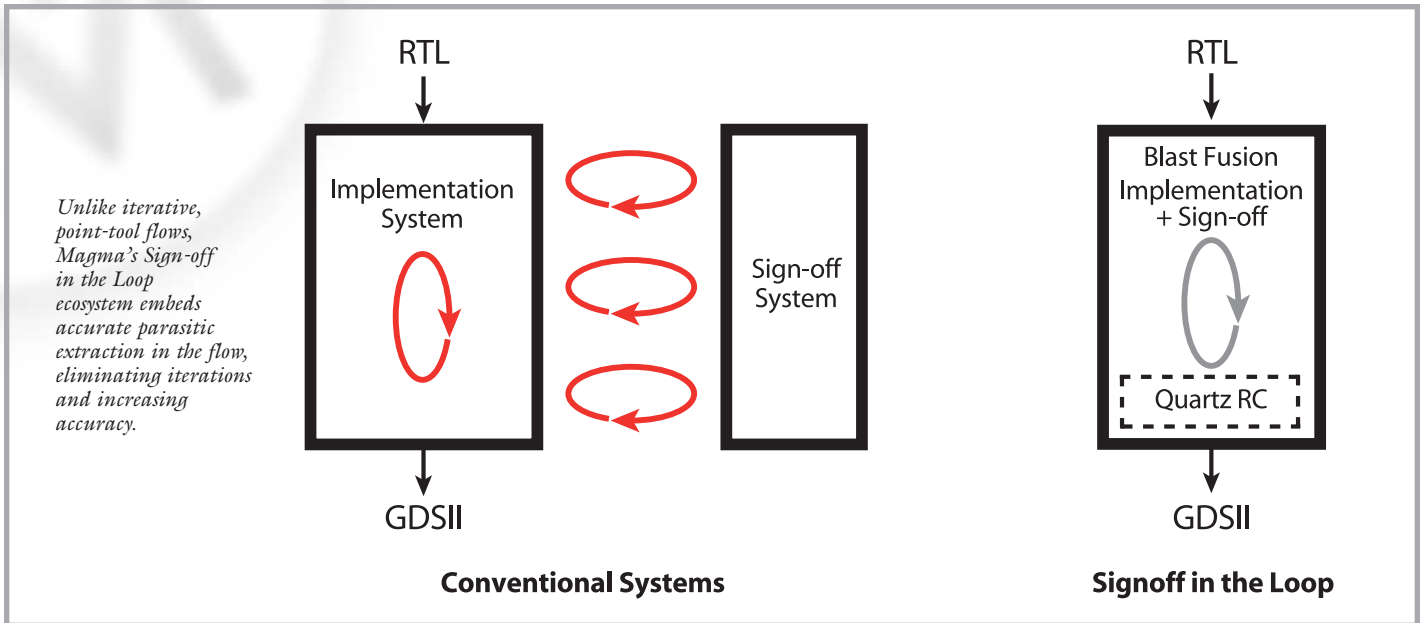
- Enables an accurate, correct-by-construction timing and noise optimization flow for the integrated Sign-off in the Loop ecosystem.
- Eliminates re-spins by accurately predicting silicon behavior with an average error rate of less than 2 percent compared to QuickCap.
- 3D capacitance rules leveraging QuickCap enhance the accuracy and robustness of Quartz RC.
- Easy to use and includes a tight integration with QuickCap for critical net extraction, combines the speed of a full-chip extractor and the accuracy of a 3D extractor to improve chip performance.
- Supports advanced 65-nm process requirements such as in-die process variations, optical and copper effects, and complex dielectric stack-ups.
- Qualified by major foundries.

Quartz RC is a 3D full-chip parasitic extractor and a key component of the Sign-off in the Loop™ ecosystem. When used in conjunction with Magma's RTL-to-GDSII design flow, it provides a correct-by-construction flow with the accuracy of QuickCap®.



In 90-nanometer (nm) and more advanced processes, interconnect delay has the most influence on accurate timing analysis, making accurate parasitic extraction of the interconnects essential. In addition, process variations and noise-inducing cross-coupling capacitances have an increasing impact on design performance. Traditional design flows include a standard physical design implementation and a separate, higher-accuracy standalone verification flow. With the increased capacitances and tighter design requirements for 90- and 65-nm designs, designers can no longer rely upon traditional, time-consuming iterative implement-analyze-repair methodologies.

Quartz™ RC



Quartz RC, part of Magma's Sign-off in the Loop ecosystem, integrates signoff-quality extraction data within the implementation phase. It allows designers to reach timing closure faster by utilizing signoff-accurate extraction data for timing and noise optimization and dramatically reduces design turnaround time. This approach eliminates external signoff iterations and delivers correct-by-construction results, reducing signoff to a mere checklist activity.

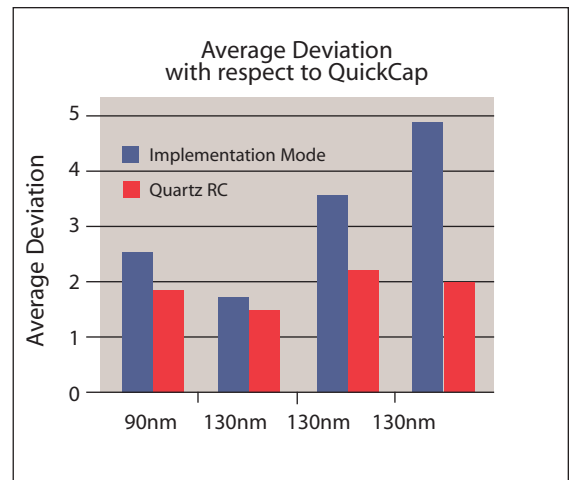
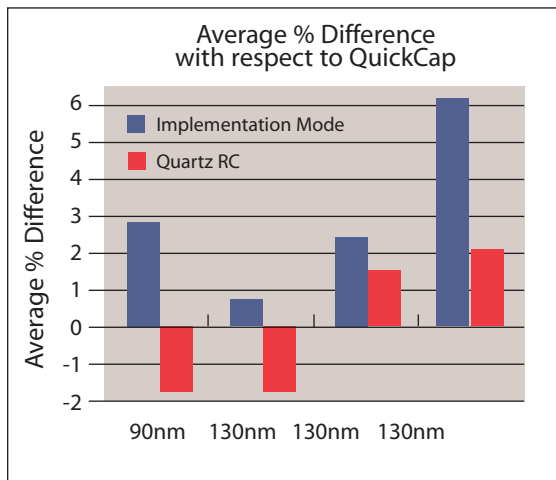
Quartz RC's average error rate is less than 2 percent compared to the industry-standard 3D extractor QuickCap. Its advanced process modeling for nanometer technologies, accurate pre-computation of the capacitances associated with interconnect structures using QuickRules™, and a highly accurate aggressor-detection algorithm makes Quartz RC a signoff-accurate full-chip parasitic extractor.

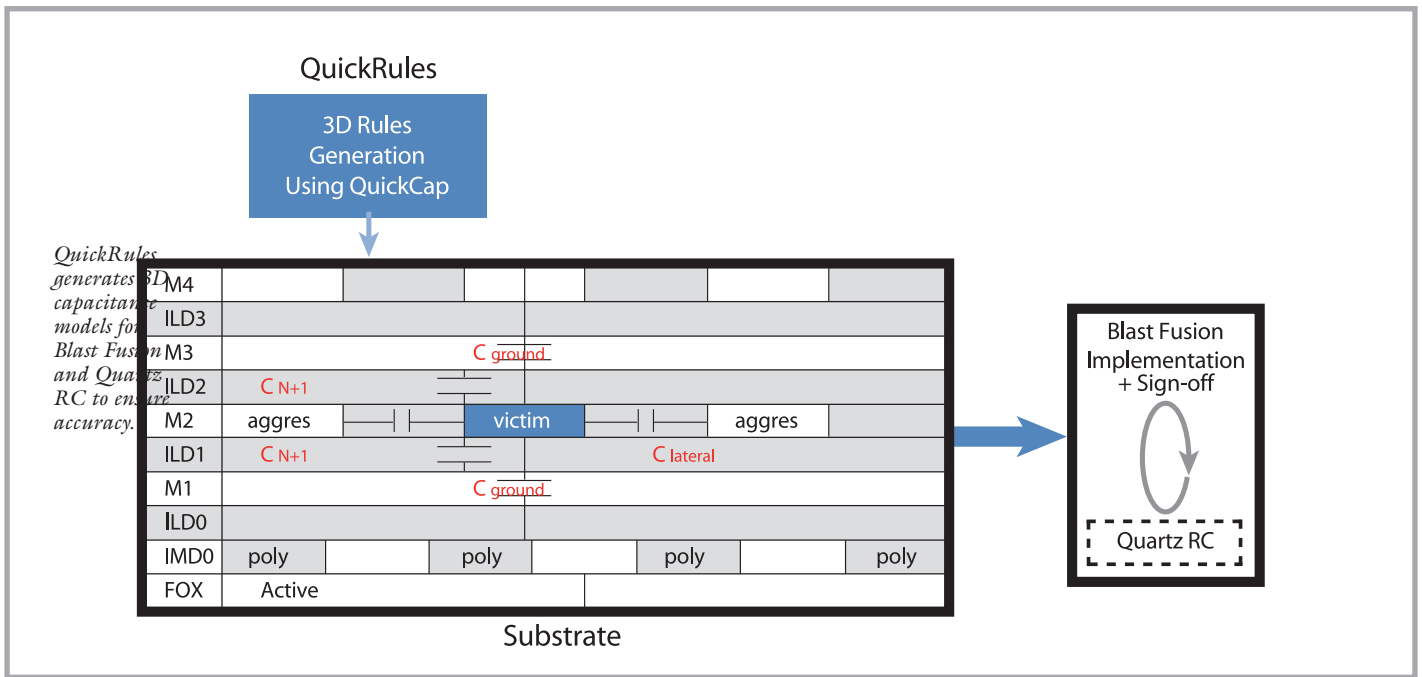
Extraction Technology

Quartz RC's extraction technology is based on pattern-matching context-based extraction. It is not just approximating but exactly performing the extraction based in the context. It has the capability to do hierarchical extraction in black-box, gray-box or white-box modes.

- For total capacitance, its results are within +/- 5 percent of QuickCap for nets above 10fF, and for nets below 10fF its results are within 10 percent or 1fF, whatever is greater.
- For coupling capacitance, its results are within +/- 15 percent of QuickCap for nets above 10fF and the capacitance ratio with respect to the total is above 10 percent.

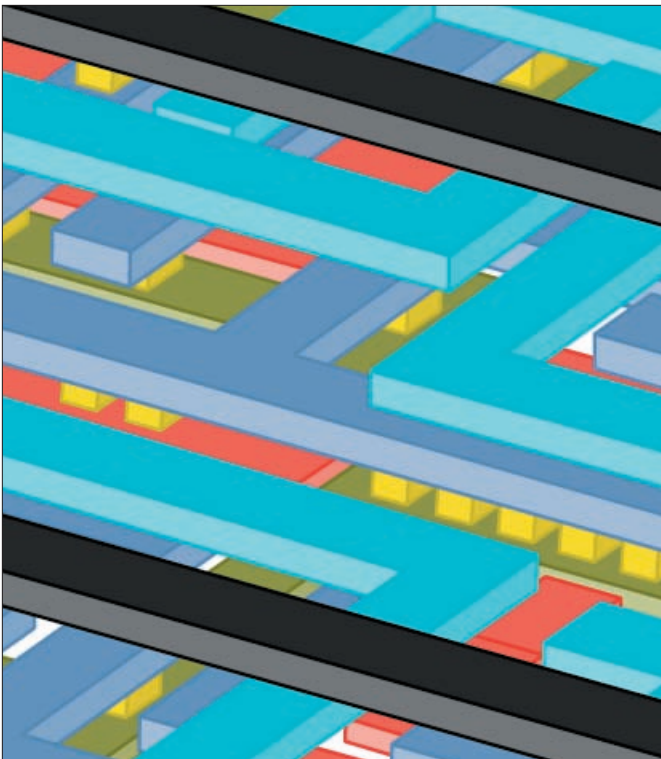
Quartz RC's average error rate and standard deviation for 90-nm and 130-nm designs is less than 2 percent with respect to QuickCap.





QuickRules generates 3D capacitance models for Blast Fusion and Quartz RC to ensure accuracy.

Unlike implementation extractors that use fixed ground planes for throughput, Quartz RC uses an automated ground plane positioning algorithm based on the metal density of the layers above and below to calculate the total and coupling capacitance.



3D interconnect model delivers accurate cross-coupling capacitance.

Fast Setup with QuickRules

Quartz RC's 3D capacitance models are generated using QuickRules, a specialized version of QuickCap. Consistency of the capacitance models is maintained by utilizing the same capacitance models generated by QuickRules in the implementation mode and Quartz RC. This ensures the predictability of the results from both these extractors. Advanced process modeling for deep submicron technologies is emerging and Quartz RC is ready. It already has the capability to model optical, copper and CMP effects which can vary depending on thickness, density, spacing and width. It also handles highly complicated dielectric stack-ups and metal fill.

Quick Link to QuickCap

Quartz RC includes the capability to initiate QuickCap for critical net extraction. This feature provides more accurate extraction for critical paths that dictate the chip's performance. Using this embedded technology designers can do on-the-fly extraction of the critical nets with QuickCap accuracy, the gold standard for capacitance extraction. Because it's built in, the design never leaves the implementation design environment and timing and noise optimization can be done with silicon accuracy and the fastest turnaround time.

Transistor-level full chip extraction can also be performed with the Quartz LVS interface to QuickCap and Quartz RC.

Quartz™ RC

Accuracy for Complex Coupling

Cross coupling capacitance is typically underestimated, which leads to inaccurate noise analysis. In Quartz RC, cross coupling capacitance is corrected using a 3D model, which accounts for accurate cross-over and cross-under. Quartz RC uses an advanced region query which does accurate neighbor searching for aggressor detection. The region query window size is determined by the coupling distance, which enables accurate, signoff quality crosstalk analysis.

Increased Throughput

Quartz RC includes key capabilities for increased throughput:

- Simultaneous multi-corner extraction provides tremendous runtime improvements over running each corner separately.
- After the ECOs, the incremental extraction engages automatically, saving additional runtime.
- For better post-extraction analysis, Quartz RC supports extraction of multiple formats simultaneously, such as a SPEF and DSPF netlist.
- A multi-threading capability is also included that linearly accelerates performance.

TECHNOLOGY FEATURES:

- Accurate full-chip parasitic extraction
- 3D capacitance rule generation
- QuickCap CNE
- Faster runtime with multi-threading
- Simultaneous two-corner extraction to reduce turnaround time
- Black-box, gray-box or white-box extraction modes
- Outputs multiple formats
- Hierarchical extraction
- Incremental extraction
- Via capacitance

Inputs

- Lef/Def, GDSII, Volcano

Outputs

- SPEF, DSPF, Volcano

Platforms

- 64-bit Solaris, 32- and 64-bit Linux

