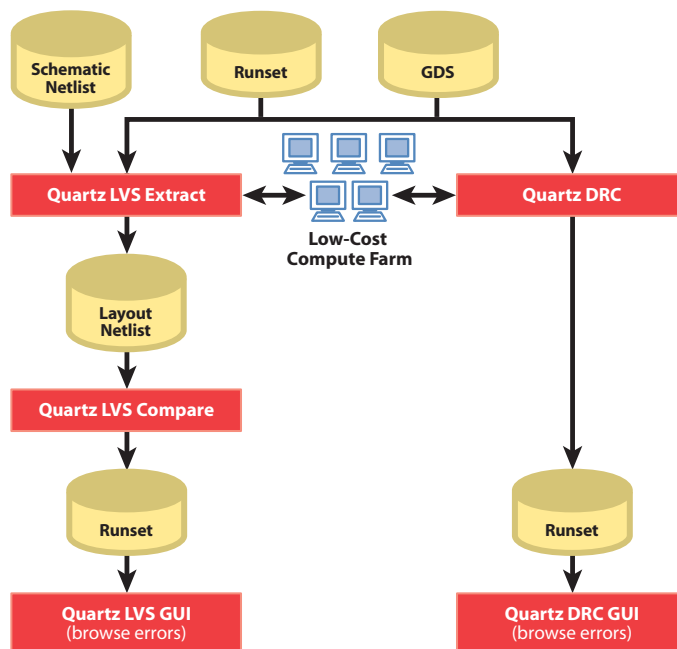


# Quartz™ DRC and Quartz LVS

- Fully scalable architecture allows any design to run in a few hours, regardless of design size or technology node.
- Memory-controlled architecture enables affordable distributed computing on low-cost Linux machines.
- Tcl runset language and graphical runset debugger provide programming power and unmatched productivity.
- Key productivity improvements provide for density, fill, antenna checking, rule-based yield scoring and short-finding utilities – reducing day-long or week-long tasks to hours or minutes.
- Native integration with Talus® and Titan™ allows for in-the-loop incremental DRC, speeding time to tapeout – greatly improving design productivity.
- Proven at major foundries worldwide with fully qualified runsets available.

Quartz DRC and Quartz LVS are the industry's first and only fully scalable physical verification solutions. Leveraging a unique architecture and advanced modeling capabilities, these revolutionary products allow affordable massively distributed processing of DRC and LVS. With this technology and the right number of processors, virtually any design can be physically verified in a few hours.



At 90 nanometer (nm) and below, there is a sharp increase in the size of designs and the complexity of design rules. These issues become even more severe at 65 nm because manufacturability concerns, primarily lithography effects, increase checking complexity. As a result, traditional physical verification architectures are no longer sufficient to address the performance demands of today.

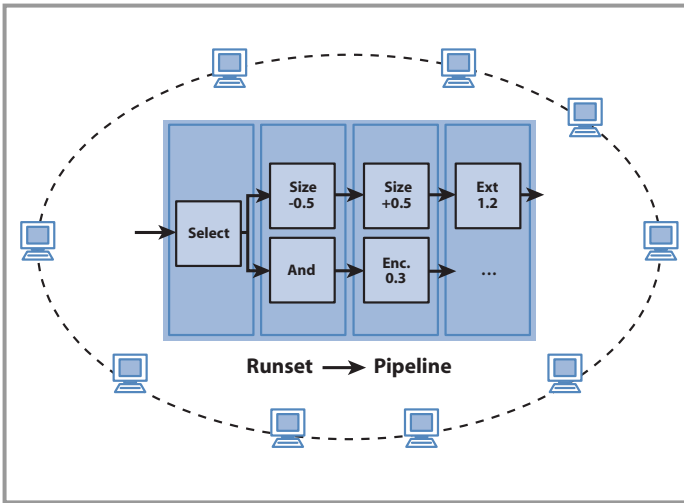
Quartz DRC and Quartz LVS are revolutionary new tools architected around two major premises. Designs at 90 nm and below need to have a scalable solution that makes effective use of available Linux compute farms to overcome the increases in design size and complexity of today's designs. Quartz DRC and Quartz LVS were designed with this requirement in mind.

# Quartz DRC and Quartz LVS

## Pipelining Breaks the Scalability Barrier

In Quartz DRC and Quartz LVS, a pipelined architecture utilizes standard compute farms and multicore-CPU architectures to perform massively distributed processing, improving both turnaround time and capacity by more than 10x.

Using this architecture, the physical verification problem is automatically split into smaller, independent tasks, making it easy to keep a farm of Linux machines busy. This fine-grain parallelism is superior to the crude parallelism available with legacy tools, and enables linear scaling well past other tools. This enables linear acceleration as the number of CPUs increases, allowing a design team to specify the desired turnaround time for physical verification in the design cycle.

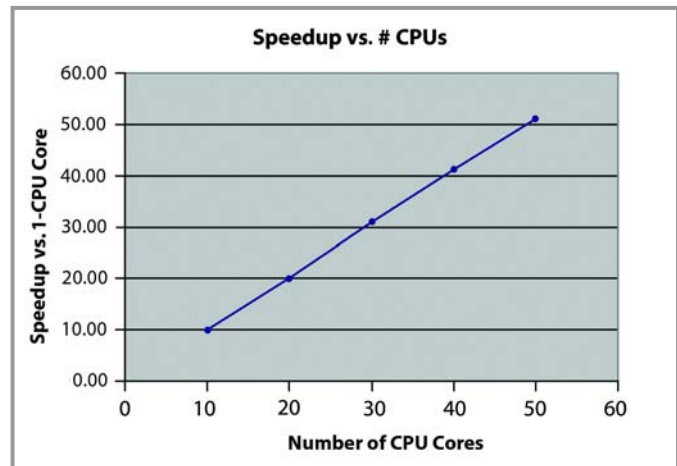


*The pipelined architecture enables massively distributed processing, which improves both turnaround time and capacity by more than 10x.*

## Affordable Computing with Memory-Controlled Architecture

Traditional physical verification tools can only make effective use of a single machine for DRC and LVS. They also require a tremendous amount of shared RAM to service the hierarchical requests from the CPUs. As a result of growing design sizes, the cycle time for physical verification has consistently increased and so has the need to use more expensive computers.

With the ability to break the physical verification process into many smaller tasks, Quartz DRC and Quartz LVS can efficiently and effectively run on very low-cost computers. Designs can be run on a single CPU, a single machine, multiple machines and multiple CPUs – the performance is linearly scalable based on the number of CPU cores used, regardless of whether they are on the same machine or not. Designers are able to leverage low cost Linux machines to enable quick turnaround times – even large designs can be done in a few hours – with the number of CPU cores varying from 8 to 16 to 32 to 64, etc., depending on design size. The sky is the limit with Quartz.



*Physical verification accelerates linearly as the number of CPUs increases.*

## Increased Productivity with Tcl Programmable Input

Quartz DRC and Quartz LVS are the first physical verification products with an open Tcl interface and provide unparalleled ease of use and functionality. Using Tcl scripts designers can program the input, runset and output. These fully programmable runsets are small, easy to read and easy to maintain.

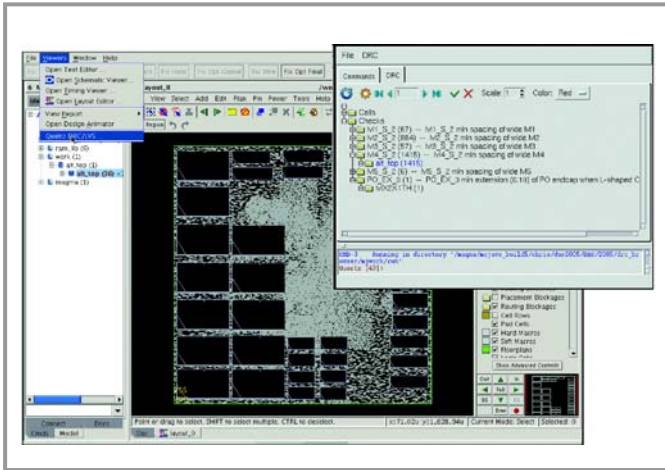
The database of results is also fully accessible through Tcl. Quartz DRC and Quartz LVS commands that access that database are provided in Tcl code, allowing designers to modify or enhance the commands. For example, all DRC error reporting is done through Tcl routines that can be easily configured to support any output format. This capability makes it easy to integrate Quartz DRC and Quartz LVS into existing flows.

## Seamless Integration with Talus and Titan

Traditional design flows run physical verification after physical design is complete. Such a flow works well if the design rules are simple – as with processes at 180 nm and above.

At advanced nodes, the iterations between physical design and physical verification cost time and effort. Costly manual ECOs are needed to fix errors that should be caught earlier – primarily due to the inaccuracy of the abstract view for design IP (standard cells, memory, I/O cells, analog/mixed signal cells) necessary for place-and-route software.

Quartz DRC and Quartz LVS are fully integrated into the Magma design implementation tools. In a single command, designers can invoke Quartz DRC and Quartz LVS from within the design environment. The Volcano™ database is read and merged with reference library GDSII files, and then the results are imported back into the design environment for viewing and fixing.

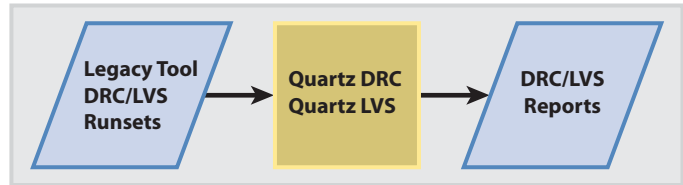


*Quartz DRC and Quartz LVS error browsing is completely integrated into the Talus and Titan implementation environments.*

This flow can be used for in-the-loop verification during the design phase. This eliminates iterations between verification and sign-off, and enables automatic ECOs to be performed in the place-and-route database.

For Talus users, Talus qDRC and Talus qLVS are options that provide Quartz DRC and Quartz LVS capabilities within the Volcano environment.

from all major foundries. Quartz also provides support for runsets from legacy tools, which is helpful for customers migrating from less efficient tools to Quartz.



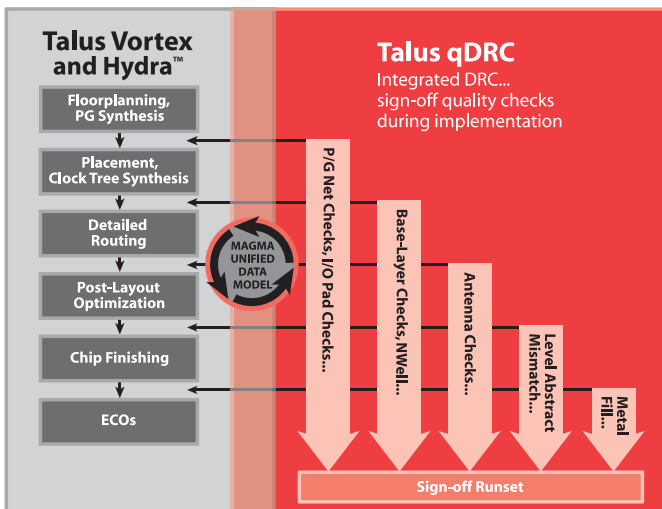
*Legacy runset compatibility greatly reduces cost to deploy Quartz in existing flows.*

### Complete Debug Environment

The DRC, LVS and LPC GUIs provide a full suite of error browsing capabilities. The GUI interfaces to Magma's Talus and Titan design systems and popular third-party layout editors. Errors can be organized by cell or by error type and can be marked as either fixed or ignored.

The short-finding capabilities within Quartz DRC and Quartz LVS are built on a unique approach that provides very fast and accurate diagnosis of the location of the short circuit. Multiple short circuits can be found in a single run and the results are immediately available within the GUI environment.

The LVS GUI has many unique capabilities that provide ease of use and speedy debugging. All LVS results are organized and presented to guide the designer to a quick and intuitive understanding of the results and the best method to begin fixing any errors. The GUI can render any portion of the layout or schematic as a schematic, making it faster and easier to visualize connectivity differences and pinpoint areas that need detailed analysis.



*Talus qDRC integrates DRC/LVS capabilities into the Talus platform, reducing the tapeout cycle by 1 to 2 weeks*

An additional benefit of an integrated flow is that certain chip finishing operations – such as pattern based metal fill – can be brought into the design flow. This capability ensures timing convergence. The traditional flow (doing pattern fill after place and route) exposes designers to the risk of timing and noise issues that must be manually fixed, if detected after chip finishing at the GDS level.

### Compatibility with Industry Standards

Quartz DRC and Quartz LVS provide native runset support

### TECHNOLOGY FEATURES

- Full set of geometric processing capabilities based on the pipelined architecture
- Built-in model-based lithography simulation and lithography hotspot repair (requires Quartz DFM license)
- All reporting done through user-visible Tcl routines for easy customization
- Single GUI for DRC, LVS and LPC with full interface to Talus, Titan and third-party layout tools
- Integrated execution from within the Talus and Titan design environments
- Direct support for foundry runsets
- Direct read of legacy tool runsets capability
- Supports LSF, Sun GRID and "rsh" job distribution

### Inputs

- Layout: GDSII, OASIS, Volcano
- Netlist: Verilog or SPICE
- Runset and extension language: Tcl

### Outputs

- GDSII, SPICE and Tcl accessible cross-reference database

### Platforms

- Linux
- AIX

MAGMA DESIGN AUTOMATION

# Quartz DRC and Quartz LVS



1650 Technology Drive, San Jose, CA 95110 USA | Tel: 408-565-7500 | Fax: 408-565-7501 | [www.magma-da.com](http://www.magma-da.com)

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