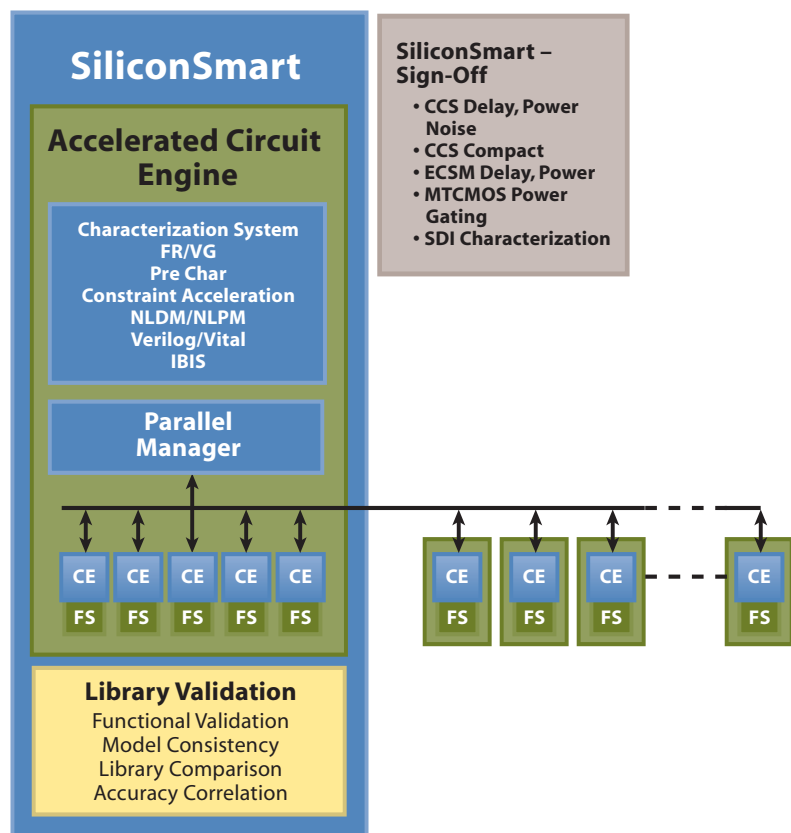


SiliconSmart[®] Sign-off

- Embedded FineSim™ SPICE ensures most accurate and fastest throughput in characterization.
- Provides fastest and most reliable path to advanced sign-off models for all major design flows.
- Characterizes CCS and ECSM current source models for highly accurate timing in sub-90-nm technologies.
- Generates the most accurate power models available, including CCS power and multi-rail extensions.
- Generates models for Quartz™ Rail transient analysis that enable power-grid-integrity analysis and repair.
- Generates noise models, including Liberty and CCS.
- Provides pessimism reduction by modeling glitch propagation and AC noise immunity.
- Supports standard cells, complex standard cells and I/Os for all features.

The Sign-off extensions to the SiliconSmart characterization system enable advanced modeling constructs for the timing, power and noise analysis and repair flows required at 90 nanometers (nms) and below. Backed by Magma's industry leading software, support and methodology, this advanced characterization system allows designers to tape out leading-edge process and low-power designs with confidence.



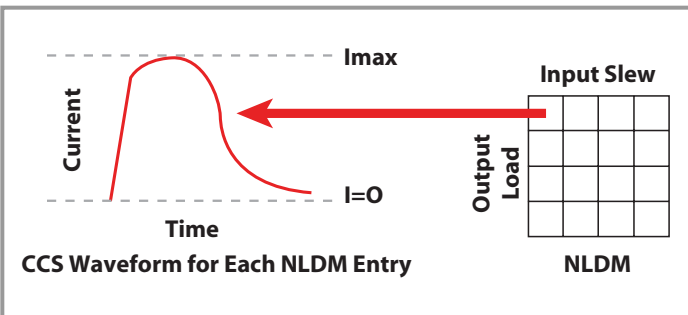
SiliconSmart Sign-off provides advanced library characterization and modeling capabilities for designs targeted at 90-nm and finer process technologies. This extension supports the latest modeling formats such as composite current source (CCS) and effective current source model (ECSM) for timing, power and noise. Current source models maintain accuracy by capturing the full output waveforms under varying slew and load conditions instead of a single delay and output slew value. Glitch characterization is also included to ensure correct logical behavior in technologies where coupling capacitance is a significant issue. Transient characterization of standard cells and power gating cells allows validation of the integrity of the power and ground network which is especially important for low-power chips.

SiliconSmart® Sign-off

Current Source Models

CCS and ECSM formats are industry standards that preserve static timing analysis accuracy in situations where wire delays constitute a significant portion of total delay. These situations are likely to arise more often in 90-nm and finer process technologies.

To model characterization data in these formats, SiliconSmart Sign-off captures a complete time dependent current (CCS) or voltage (ECSM) waveform for each input slew and output load value combination instead of the single delay value that goes into a NLDM (non-linear delay model). In addition, the input capacitance value is captured for each input slew and output load value combination instead of a single capacitance value for the whole table in the NLDM scheme. The detailed waveform and input capacitance characterization allow a static timing analysis tool to more accurately compute the delay through the driver and parasitic load combination.

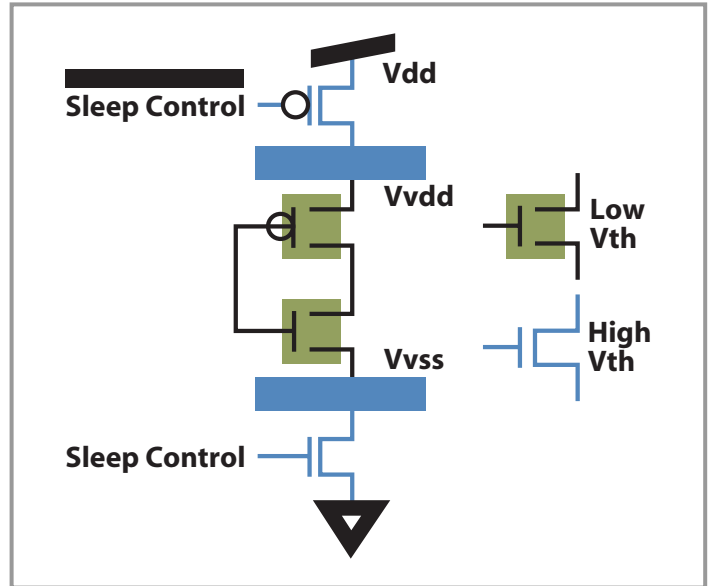


For CCS modeling, a current waveform is generated for each NLDM entry.

Advanced Low-Power Models

Transient rail (power and ground network) analysis is becoming increasingly important in low-power designs. Static rail analysis is unable to analyze time domain spikes in the power and ground nets or determine how much decoupling capacitance must be added to bring the spikes within specification. For designs in which blocks can be powered down, it is also important to determine power-up times and maximum current draw during power-up in order to maintain power supply adequacy. Magma's Quartz Rail transient analysis can answer these questions. Transient analysis entails characterizing current waveforms and determining the intrinsic decoupling capacitance and series resistance for every library cell. In addition, the IV curve for MTCMOS switch cells must be characterized. SiliconSmart Sign-off performs these characterizations and

supports both the industry-standard CCS power format and the Magma input format. The latter enables seamless use with Quartz Rail transient analysis.



SiliconSmart Sign-Off characterizes the IV curve for MTCMOS switch cells.

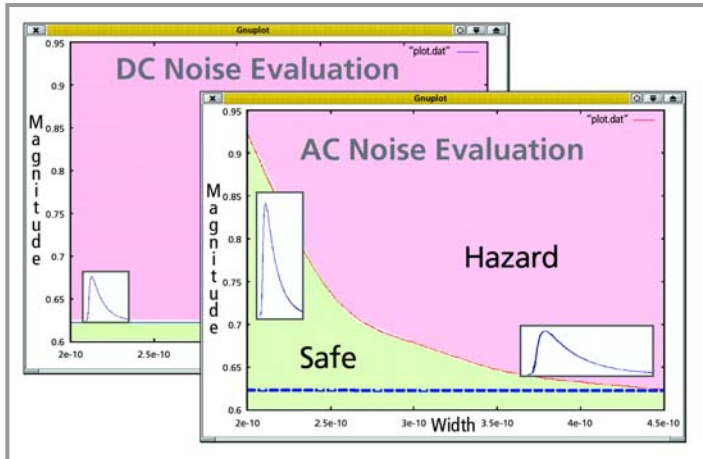
Noise Characterization

In the area of glitch noise analysis, SiliconSmart Sign-off supports both the highly accurate CCS modeling and traditional Liberty modeling.

The CCS model captures instantaneous current for every combination of input voltage and output voltage values for the input and output channel-connected transistor stages of every standard cell. This enables computation of both induced and propagated glitches and an easy determination of functional failure by computation of the accurate glitch at flip-flop feedback nodes. This allows the prediction of flip-flops entering incorrect states.

In the traditional Liberty modeling scheme, there are three distinct parts. One is the measure of a cell's capacity to withstand glitches by determining its drive resistance in the steady states of both high and low. This resistance, known as holding resistance, may be characterized in the form of an IV curve. In addition, it is necessary to know what glitch height and width combination or AC margin (or, for more pessimistic calculations, just the glitch height – DC margin) a cell can withstand before toggling to a false state. Finally, the actual impact of glitch noise can only be determined by understanding whether a particular glitch can be captured

in a flip flop. Noise propagation characterization assists with this by characterizing the noise amplifying or attenuating effect of each cell. This feature can help to significantly reduce pessimism and thereby over-design. SiliconSmart Sign-off characterizes all of these properties in Liberty format.



Characterizing AC noise margins greatly reduces pessimism by allowing tall by narrow noise glitches.

TECHNOLOGY FEATURES:

Measurements

- ECSM and CCS
 - Driver model
 - Time-dependent voltage or current waveform for every input slew and output load value combination
 - Receiver model
 - Input pin capacitance for every input slew and output load value combination
- CCS Power and Quartz Rail Transient
 - Time-dependent current waveform at supply pin for every input slew and output load value combination
 - Intrinsic decoupling capacitance and series resistance characterization for every input slew and output load value combination
 - IV curve characterization of MTCMOS power switch
- CCS Noise
 - Instantaneous current for every combination of input voltage and output voltage values for the input and output channel-connected transistor stages
- Liberty Noise
 - Holding resistance (or IV curve)
 - AC and DC noise margin
 - Models hazardous glitch energy
 - Applicable to comb. and seq. arcs
 - Noise margin, rejection and immunity curves
 - Height and width with respect to cap load
 - Noise propagation tables
 - Propagated height/width with respect to input height/width/cap load

Model Views

- CCS timing, power and noise
- Compact CCS timing and power
- ECSM
- Quartz Rail low-power transient analysis model

Platform Support

- Linux (Red Hat)

Supported SPICE Simulators

- FineSim SPICE
- HSPICE
- Spectre
- Eldo

MAGMA DESIGN AUTOMATION

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