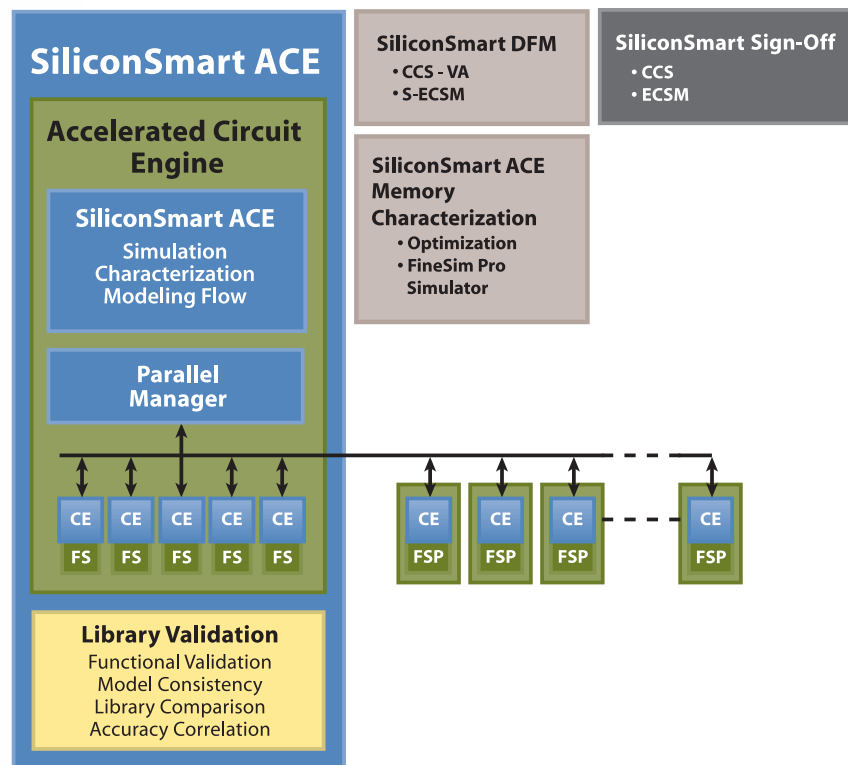


SiliconSmart[®] ACE Memory Characterization

- FineSim[™] Pro simulator enables the optimal tradeoff between accuracy and performance for different portions of the memory circuit.
- Advanced simulation technology in FineSim Pro, such as non-ideal power analysis and RC reduction, makes SiliconSmart ACE Memory Characterization a simulation-friendly tool.
- Generates the most accurate memory models from 100% FineSim Pro simulation-based measurement data.
- Advanced, FineSim Pro assisted characterization methodology optimizes memory circuit simulation and model generation.
- The parallel job manager intelligently distributes FineSim Pro simulation across a computer network to achieve the highest throughput gains.
- SiliconSmart ACE Memory Characterization's easy setup enables quick re-characterizations of compiler created instances and creation of more accurate models.
- Embedded FineSim Pro simulator makes SiliconSmart ACE Memory Characterization a cost-efficient solution.

SiliconSmart ACE Memory Characterization is an extension to the SiliconSmart ACE product line. It enables the characterization and modeling of memory instances with complete simulation-based accuracy and unprecedented throughput by leveraging Magma's accurate, high-capacity and ultra-fast FineSim Pro simulator.



One of the challenges in today's system-on-chip (SoC) designs is the ever-increasing circuitry sizes. Along with new and additional functionality, more and more embedded memory instances are being incorporated into a single chip. These memory instances not only consume a large portion of silicon real estate, they also use more power and increase timing latency on critical paths. A design flow with accurate library models for standard cells and I/O pads is no longer enough to achieve design closure. That's because a bad model in a memory instance can easily result in inaccurate timing analysis and wasted effort in building an accurate standard-cell library. It is critical for a design team to have accurate models for all IP libraries generated by a tool flow that has a consistent and accurate timing, power and noise characterization methodology.

SiliconSmart[®] ACE Memory Characterization

Typically, a memory instance is generated by a memory compiler, which includes design netlist, physical layout, and electrical models. A memory compiler builds up its own database for modeling by simulating a very limited number of memory instances, usually a smallest, a largest and a few sizes in the middle. For a newly created instance that is not on this short list of samples, the memory compiler uses a data manipulating technique such as interpolation and extrapolation to fit certain polynomial equations. It is inevitable that this approximation leads to inaccuracies in its models. Even for an instance that has been simulated in a compiler data base, its operating process, voltage and temperature (PVT) condition might have changed, invalidating the previous model's accuracy. Eliminating this inaccuracy in generating a memory instance model requires a memory characterization tool that can re-characterize such instances accurately and quickly.

The efficiency and accuracy of a characterization tool relies largely on the efficiency and accuracy of the simulator it invokes. This is especially true in memory characterization because memory circuits are hundreds of thousands of times larger and require longer transient simulation windows than standard cells. Lacking simulation power, traditional memory characterization tools use estimations such as static-path-delay-based circuit reduction and data interpolating for large setup/hold look-up table creation. Such corner-cutting tricks defeat the purpose of re-characterizing a memory instance because these traditional tools deliver the same level of accuracy as a memory compiler. Empowered by Magma's FineSim Pro simulator, SiliconSmart ACE Memory Characterization has the ability to simulate all arcs on all data points, including time-consuming setup/hold points, and to create the most accurate memory models.

FineSim Pro Simulator

FineSim Pro is the industry's only simulator that has both SPICE and fast SPICE integrated into a single executable. This combination provides the best tradeoff between accuracy and performance and is well-suited for memory designs because different modes can be applied to different portions of the memory circuit, depending on the level of accuracy required. For example, analog circuitry such as sense amps can be run in SPICE and control logic in fast SPICE. For memory circuits with multiple power domains, SiliconSmart ACE Memory Characterization can use FineSim Pro's non-ideal power-rail analysis feature for better circuit partitioning and RC reduction among active devices, for signal RC as well as power rail RC networks and to achieve the best simulation results.

Dynamic Circuit Reduction

It's common for a memory circuit to have millions of elements in its post-layout netlist, and a full characterization set has tens or even

hundreds of simulation decks. Unlike a functional simulation that fully verifies a memory behavior, a characterization stimuli or vector set only simulates a specific portion of the circuit for a required measurement type. SiliconSmart ACE Memory Characterization uses FineSim Pro to do a fast simulation to monitor and record inactive nodes. After a subsequent structural analysis to identify an inactive channel connected region (CCR), SiliconSmart ACE Memory Characterization does a smart netlist pruning and selectively back-annotates RCs onto this pruned netlist. This dynamically created netlist per vector set greatly reduces the size of the whole simulation deck and accelerates the simulation in characterization.

Automatic Internal Node Identification

For a memory circuit's "write" operation, data and clock meet at an internal latch node. This requires its setup/hold measurements to be done on this internal node. It's difficult to identify such internal nodes, especially when the netlist is totally flat and fully RC extracted. SiliconSmart ACE Memory Characterization uses FineSim Pro to monitor and record toggles on nodes where the data and clock meet. After a thorough heuristic analysis, SiliconSmart ACE Memory Characterization filters potential candidate nodes based on whether nodes toggle or not with large constraint margins in "pass" and "fail" conditions, and then automatically selects the right one for setup/hold measurements.

Constraint Acceleration Technology

Similarly to standard-cell characterization, constraint measurements such as setup/hold are time-consuming and a throughput bottleneck. In addition to all the constraint acceleration technologies used in SiliconSmart ACE standard-cell characterization, the memory characterization extension employs unique technology to further speed up measurements in a memory circuit. This technology uses FineSim Pro to initialize a memory circuit and selectively save its states in the first clock cycle, and then intelligently re-uses them for the second clock cycle when constraint measurements are taken.

Template-Assisted Ease of Setup

SiliconSmart ACE allows the user to import a known .lib file to keep its Liberty format structure in a re-characterization flow. For a memory re-characterization, however, this is not enough because, unlike the trivial setup required for a simple NAND gate, setting up a function and vector for a memory circuit is tedious and often troublesome. SiliconSmart ACE Memory Characterization supplies a template library to describe functions for commonly-used memory types. This high-level functional description automatically creates all control files and all the necessary simulation vectors on all the arcs. When combined with the structure in the existing .lib, SiliconSmart ACE Memory Characterization is able to create the same structure in .lib using accurate numbers from the FineSim Pro simulation.

TECHNOLOGY FEATURES:

- Embedded or standalone FineSim Pro simulator
- Parallel job manager to distribute FineSim Pro simulations over a LSF/SunGrid network
- Consistent SiliconSmart ACE flow, methodology, platform, input and output format
- Dynamic circuit reduction through smart netlist pruning
- Selective RC reduction and back annotation
- Automatic internal node identification for constraint measurement
- Constraint acceleration technology
- Automatic re-characterization flow with template-assisted characterization setup, including vector generation
- Ability to supply user-defined vectors through an add-user-stimulus (AUS) description

Applications

- SRAM
 - Synchronous / Asynchronous
 - Single-port / dual-port
- REG file
 - Single-port / dual-port
- ROM



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