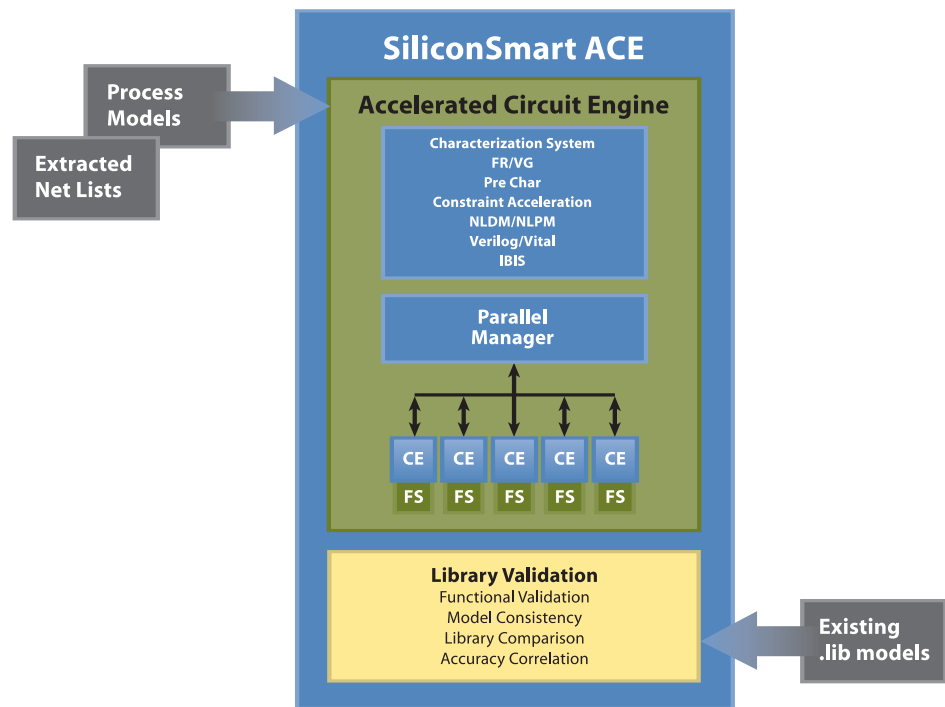


SiliconSmart[®] ACE

- Embedded FineSim SPICE ensures most accurate and fastest throughput in characterization.
- Automatic function recognition and vector generation ease set up of library characterization, including complex custom and I/O cells.
- Pre-characterization and constraint acceleration optimizes and minimizes required simulation decks.
- Advanced constraint acquisition methodologies deliver highest accuracy and flexibility of setup/hold measurements.
- Adaptive parallel job manager leverages an unlimited number of CPUs to provide throughput scalability, delivering unrivalled performance utilizing the highest level of parallelism (on an arc-by-arc basis).
- Generates accurate traditional non-linear models and advanced CCS, ECSM models to prevent silicon re-spins.
- Provides fast turnaround of library models for any new process model updates and supports custom PVTs through the re-characterization flow.
- Generates Verilog and Vital/VHDL models back-annotated with SDF from Liberty models to enable gate-level simulations.
- Supports a wide variety of both industry-standard and customer-proprietary simulators.
- Includes IBIS models for I/O cells.
- Models easily integrate with all popular design flows.
- Provides base platform for SiliconSmart Sign-Off and DFM Extensions.
- Features low cost of ownership.

Featuring industry-leading accuracy, throughput and ease of use, the SiliconSmart tool suite provides standard-cell, I/O, custom macro, and memory characterization and modeling for all popular design flows. It supports all the advanced timing, power, noise and statistical modeling specifications. The proprietary Accelerated Circuit Engine (ACE) fully automates the characterization flow, employing the most advanced circuit function recognition technology and vector generation and optimization algorithms to efficiently characterize cells without compromising accuracy.



For maximum performance, SiliconSmart ACE embeds Magma's accurate and ultra-fast SPICE simulator, FineSim™ SPICE and improves the total throughput by up to an order of magnitude. SiliconSmart ACE sets a new standard by providing the most reliable and shortest path to high-quality, production-ready Composite Current Source (CCS) models or Effective Current Source Models (ECSMs) for timing, power and noise for 28-nm and finer processes.

SiliconSmart[®] ACE

Library developers, IP vendors and COT design teams rely on abstract models to accurately represent the electrical behavior of circuits implemented with advanced process technologies. Automated IC design flows for 45-nanometer (nm) and finer processes have given designers much greater flexibility to customize their designs. An increasingly popular technique is to include custom cells, macros, memories and I/Os that help meet design-specific goals. This also places a greater burden on library teams because they must deliver advanced CCS or ECSM sign-off models for these functionally and electrically complex circuits. Design differentiation due to changes in process corners, supply voltages and junction temperatures (PVTs) is also driving up the number of operating points that a library must support. The volume and complexity of characterization has never been higher, and will continue to grow as process technologies move to smaller nodes. To meet these challenges, the SiliconSmart tool suite combines ease of use, accuracy, faster throughput and comprehensive standard-format support, enabling designers to shorten design cycles and improve chip performance with silicon-proven library models.

Embedded FineSim SPICE Simulator

FineSim SPICE is an industry-leading, pure SPICE simulator. Its native parallel simulation technology is widely used by analog and IP designers working on the most innovated circuit designs. It has been certified by a major foundry for 65-, 40- and 28-nm process nodes, demonstrating its ability to accurately handle the latest process models. SiliconSmart ACE integrates this simulator through FineSim SPICE's C++ API and offers both a characterization engine and a simulation engine in a single executable.

With the embedded FineSim SPICE, SiliconSmart ACE eliminates the need to switch back and forth between separate characterization and simulation tools. Unlike using a standalone SPICE simulator, with SiliconSmart ACE, no time is wasted repeatedly loading in SPICE models and I/O traffic is minimized. In a single characterization session, SiliconSmart ACE executes parsing, elaboration, data sweeping and more, greatly increasing the overall characterization throughput.

Automatic Function Recognition and Vector Generation

Leveraging Magma's patented technologies, SiliconSmart ACE reads in a CMOS transistor-level cell netlist and performs static structural analysis to automatically determine functionality. Based on Channel Connected Block (CCB) partitioning and logic cone tracing between primary outputs and inputs, this analysis handles a wide range of cells, from simple standard cells to very complex custom, macro or I/O cells. Circuit topology revealed by the automatic function recognition also allows SiliconSmart ACE to generate a smart set of vectors to simulate all arcs inside a cell. This automatically generated

vector set covers all necessary stimuli without any redundancy and minimizes the number of simulations required to characterize a cell without any loss of arc coverage or model accuracy. To enable characterization of only certain cell paths, SiliconSmart ACE still supports the use of traditional user-defined functions and vector sets to guide the simulation sequence and measurement types for model creation.

Automatic function recognition and vector generation remove the dependency on a pre-defined function such as that in an existing .lib file. This automation, combined with a rich set of supported features such as differential signals and variable electrical modes in a programmable cell, provide flexibility and ease of use in setting up a successful characterization run.

Pre-Characterization and Constraint Acceleration Technology

SiliconSmart ACE can further analyze the automatically generated vector set before final simulation. This pre-characterization procedure includes sharing state-specific characterization conditions (also known as vector binning) and calling the embedded FineSim SPICE to quickly grade these vectors in the bin. Controllable by a user-defined error tolerance level, the whole set of vectors can be categorized into different bins. Only one simulation is required for a single bin. Other vectors in the same bin can be represented by the same measurement results in the created models.

SiliconSmart ACE supports a wide range of constraint methodologies, from standard design flows to leading-edge performance applications for maximizing yield and performance. For example, SiliconSmart ACE allows sampling of internal nodes in a sequential cell to look for glitches in order to remove potential optimism for setup/hold constraints. It also provides multiple ways of capturing the dependency between setup and hold checks for different design styles. The SiliconSmart ACE constraint acceleration technology shortens the traditionally time-consuming task of measuring constraints. This technology performs a structural-based analysis for sequential path sensitivity to boundary conditions, proposes an intelligent initial bi-section seeding based on slew sensitivity analysis and invokes the embedded FineSim SPICE to perform a bi-section search in a single SPICE run.

Library Validation

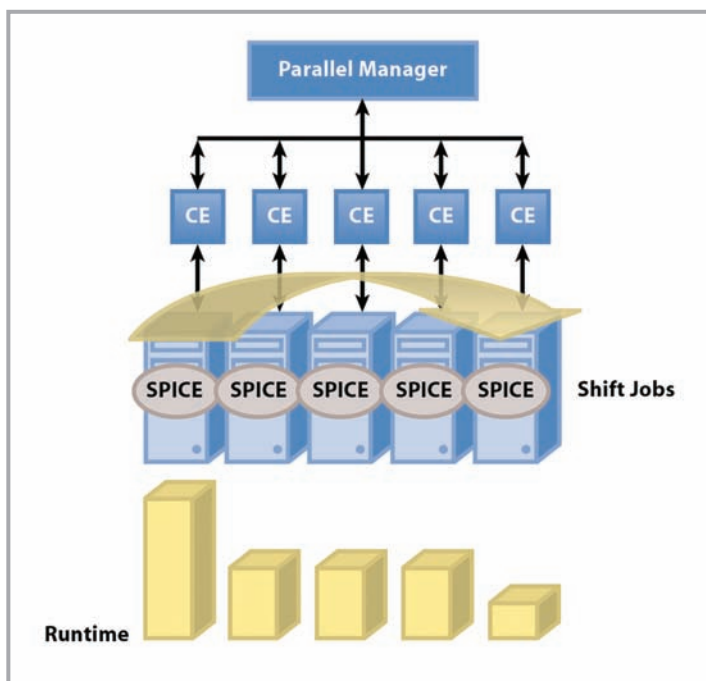
SiliconSmart ACE includes a closed-loop library validation feature that compares cell functionality and data accuracy against a pre-characterized golden library, ensuring model consistency between Liberty and Verilog formats. Other EDA tools such as a Verilog simulator can be called to validate generated models.

A library characterization run involves a large amount of data generation, collection and management. SiliconSmart ACE's data dependency manager monitors file dependency in each

characterization step and eliminates the need to re-characterize an entire library or any cell by immediately identifying which cells are affected by changes to the cell transistor netlist or SPICE model, or configuration settings. This ensures library consistency. When a minor change occurs to any input data, this also provides a huge runtime savings in the generation of accurate and production-ready library models.

Throughput Maximization by Parallelism

SiliconSmart ACE intelligently combine measurements into simulation arcs, optimizing the number of simulations and accelerating that process through parallel characterization. Its adaptive parallel job manager distributes simulations to a network of computer servers and automatically adjusts CPU loading based on CPU performance and the job queuing platform. Overall characterization throughput improvements are nearly linear with each additional CPU. The default configuration for SiliconSmart ACE supports 5 CPUs, but the user can increase this count to as many CPUs and simulator licenses as are available.



SiliconSmart ACE's adaptive parallel job manager distributes simulations to a network of computer servers and automatically adjusts CPU loading.

Customization and Accuracy Control in Power Characterization

At advanced technology process nodes, leakage power starts to dominate, making internal switching power measurement difficult. Magma's methodology guidance and advanced characterization algorithms make it easier to set up characterization with the best combination of accuracy and runtime. SiliconSmart ACE

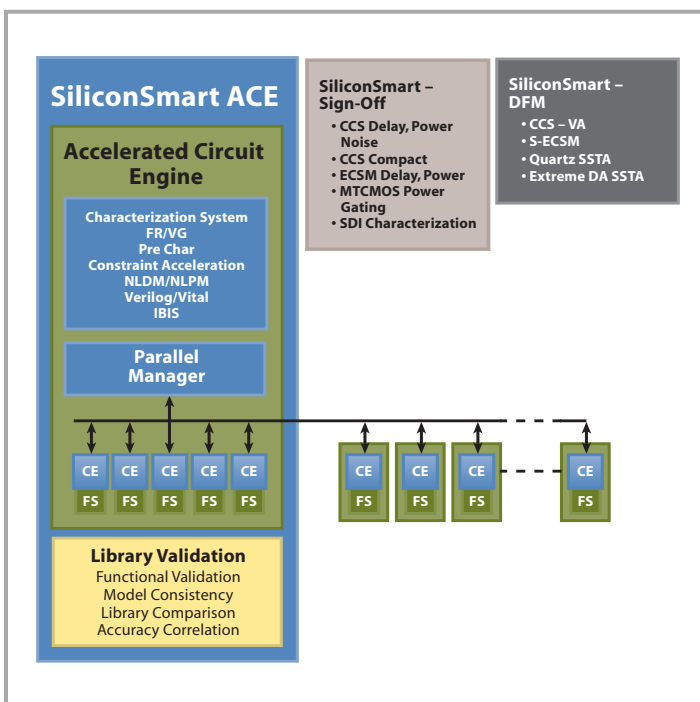
properly accounts for leakage power, external switching power, hidden power (internal switching power when output values do not transition in response to an input transition), multiple output cells and multiple power-rail cells to meet the needs of various power analysis and optimization tools for low-power designs.

SiliconSmart Sign-Off and DFM Extensions

SiliconSmart ACE provides fundamental library characterization features and capabilities. Additional extensions are also available that target specific design challenges, including sign-off and design for manufacturability (DFM).

The SiliconSmart Sign-Off Extension enables advanced modeling constructs that support the timing, power and noise analysis and repair flows that are required at 90 nm and below. They include support for the latest modeling formats such as CCS and ECSM for timing, power and noise. These models enable transient current modeling for standard cells, power-switch cells and MTCMOS cells, allowing validation of the integrity of the power and ground network for low-power chips.

The SiliconSmart DFM Extension generates statistical and process sensitivity information in variation-aware models for timing and leakage. DFM characterization identifies cells prone to performance degradation due to lithographic (systematic) or process (random) variation, enabling optimization for better yields at higher frequencies.



SiliconSmart sign-off and DFM extensions target specific design challenges.

SiliconSmart® ACE

TECHNICAL FEATURES

- Embedded FineSim SPICE Simulator
- Parallel characterization distributed on heterogeneous compute farms with unlimited CPU counts
- Supports industry-standard load sharing systems
 - LSF
 - SUN GRID
- Automatic library characterization setup
 - Automatic function recognition from SPICE netlist including state-table-based functions
 - Automatic circuit topology-driven vector generation
 - Automatic structure and/or simulation-based vector optimization (pre-char)
 - Automatic constraint acceleration technology for sequential measurements
 - Automatic characterization points and range selection
 - Automatic gathering of all data from simulation to create all model views concurrently
- Active driver or emulated driver to supply realistic, non-linear input waveform shapes to characterization
- State- and path-dependent timing and power
- Dependency management via simulation caching
- Automatically re-characterizes flow using an existing .lib file
- Tcl command line user interface

Cell Types

- Single- and multi-output combinatorial cells
- Complex latches and flip-flops, including retention flops, multi-bit flops, dual edge flops
- Electrically complex multi-voltage, bi-directional I/O cells
- Tri-state and open drain cells
- Special cells including one-hot MUX, bus keeper and clock gating
- Special I/O cells such as LVDS, USB, PGIO, DDR, PCI, SSTL

I/O Features

- Differential inputs and outputs
- Multiple voltage supplies
- User specifiable complex load networks
- Characterization of multiple electric modes per driver

Measurements

- Intrinsic delay and output transition time
- Effective input pin capacitance
- Minimum pulse widths
- Setup, hold, recovery and removal times
- Constraint edge control
 - Dependent or independent setup and hold
- Constraint violation determination
 - Functional failure
 - Absolute, relative and user-defined delay or slew degradation
 - Output and internal node glitch checking
- Leakage and internal (transition and hidden) power
- Statistical model measurements
- IBIS 5.0 measurements
 - Current and voltage curves plus different launch delay
 - On-die termination (ODT)
 - Programmable driver strength
 - Optimal point selection for static IV curve generation

Model Views

- Liberty (.lib)
 - Non-linear delay model (NLDM)
 - Non-linear power model (NLPM)
 - CCS timing, power, noise, variation-aware
 - Compact CCS
- ECSM (version 2.1.1) timing, power, statistical (S-ECSM)
- Verilog
- VHDL/Vital
- IBIS 5.0 I/O models

Validation Features

- Liberty model comparison
- Automatic Verilog/Vital functional and back-annotation validation
- Automatic STA to SPICE results correlation

Platform Support

- Linux (Red Hat)

Supported SPICE Simulators

- FineSim SPICE
- HSPICE
- Spectre
- Eldo

