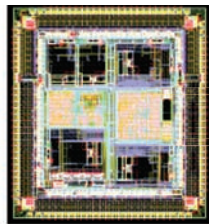


TitanTM ALX

- Dramatically shortens time and effort required to implement layout changes in sensitive analog circuits.
- Automatically handles the most complex DRC and DFM rules by leveraging a novel and proprietary layout model that supports layout abstraction, hierarchy and PCells.
- Automatically extracts and meets most analog constraints, eliminating time-consuming manual entry.

Titan Analog Layout Accelerator (ALX), an integral part of Magma's Titan Mixed-Signal Design Platform, solves today's analog/mixed-signal custom layout design migration and retargeting challenges. Titan ALX automates analog layout migration to new technologies. The migrated layouts are usually DRC clean and preserve the analog layout intent carefully expressed in the previous layout. Titan ALX improves reuse of existing high-quality circuit layouts and minimizes the number of design rule check (DRC) and design for manufacturing (DFM) errors that must be fixed by the IC mask designer. This results in significant reductions in the amount of time, effort and costs of custom layout design.

Existing Layout

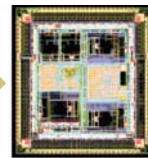


65 nm

Titan ALX

45 nm

New Layout



Today, chip designers spend most of their efforts on re-implementing a given design for new foundries, processes and technology nodes. Design specifications change, however, critical building blocks are rarely redesigned from scratch. Expert circuit designers create their circuits with future re-implementation in mind, making the circuit and layout re-implementation less costly.

Despite these best efforts, porting designs to a new foundry, technology or node is still difficult. The more advanced the node, the larger and more complex the DRC and DFM rules, and the higher the relative cost of layout re-implementation compared to circuit redesign.

With Titan ALX, implementation of most engineering change orders (ECOs) can be achieved with a fraction of the effort required by traditional custom IC mask design tools. Large changes that disturb the layout footprint and require manual intervention can be seamlessly incorporated within the Titan ALX flow, accelerating iterations between circuit and layout design teams.

Titan™ ALX

	Size	Retarget Time	
		Traditional (Person-Months/Days)	Titan
SERDES Block B1 45Fab to 45TSMC	~20k devices	16 months	1 day
SERDES Block B2 65Fab to 45TSMC	~2k devices	2 months	2 hours
VCO 130UMC to 90TSMC	~100 devices	2 days	2 minutes
VREF 130UMC to 65TSMC	40 devices	1 day	1 minute

Designers can input their GDSII into Titan, identify blocks and cells for re-targeting, and do fast path-finding studies to quickly understand the impact of new DRC and DFM rules in advanced nodes such as 45 nanometer (nm), 65 nm, 90 nm and 130 nm.

Once the impact of new DRC and DFM rules are understood and handled, designers can enter new device sizes for their analog circuits, and very quickly get a full-custom layout implementation at the new target node without having to wait for the IC mask designer to implement the changes. This helps speed up the overall design convergence by reducing the time it takes for iterations between circuit design changes and post-layout simulations.

After the circuit is converged to a 90 percent confidence level with post-layout extraction and simulation, designers can switch to a more traditional manual and hands-on methodology where original design hierarchy and process design kit (PDK) PCells are reused. This allows the mask designers to make minor modifications with less effort and time.

Titan ALX can be used to speed up the design of all custom circuits from standard library cells to datapath and memory blocks, to custom analog circuits, to full-chip layout reuse.

Titan ALX can also be combined with Titan's state-of-the-art shape-based router and fast custom block/cell/transistor placer to accelerate custom mixed-signal chip design.

Technology Features

- Migrate analog circuit layout while preserving layout beauty and design intent
- Support complex DRC/DFM rules in the most advanced nodes, including poly spacers, discrete poly rules, max-device width, conditional/corner spacing
- Automatic hierarchy preservation

- Automatic PCell creation using target node PDK
- Automatic preservation of symmetry and alignment
- Automatic or custom device sizing, including custom support for transistor folding / fingering options
- Schematic-driven device sizing
- Automatic device type changes, such as n+ resistor to OD resistor
- Designer toolbox for helping custom layout engineer during new design implementation or modifying existing layout due to ECOs
- Automatic DRC clean-up for a quick and dirty layout; go from dirty layout to DRC-clean layout instantly
- Quick design prototyping by migrating all critical design layers, including well, diffusion, poly, vias and metals
- Automatic handling of pin/pitch matching constraints - quick DRC vs. area tradeoff studies
- Flexible handling of difficult hierarchy constraints enables unimportant aspects of hierarchical layouts to be smartly relaxed to reduce DRC errors by orders of magnitude
- Flexible handling of PCell constraints, allowing automatic computation of non-default values for the layout parameters of each PCell to significantly reduce DRC errors
- Abstract and easy-to-modify rule deck used to calibrate layout
- Speed up circuit and layout effort by quick what-if experiments changing layout rules

Advanced Capabilities

- **Ease of Use**
Eliminates tedious data entry for matching, symmetry and alignment constraints. Complex layout beauty aspects are automatically extracted from existing layout and enforced in the new layout. Pre-setup rules for popular target foundries, such as any variant of TSMC's 180 nm to 45 nm processes. Use with any layout editor. Includes GUI-based layer mapping, device sizing, debugging and custom constraint specification.
- **Quality of Results**
Layout beauty is preserved while DRC and DFM errors are reduced to zero for many analog/custom circuits and very close to zero for large IP blocks. Built-in self test system compares source and target layout device and wire connectivity to assure LVS-clean output.
- **Productivity**
Migrates full layout for many tough analog and custom digital circuits in minutes. Resulting layout can be cleaned up by an expert mask designer in a few hours for large blocks, achieving orders of magnitude reduction in layout design time, effort and cost

Design Methodology

Layout Migration: Node-to-Node and/or Foundry-to-Foundry with New Device Sizes

- Import GDSII or other layout database into Titan
- Specify a layer mapping from input layout to Titan ALX layer tags using the easy-to-use Titan ALX GUI
- Specify input node, output node and scaling factor
- Specify target device sizes or just use linear scaling
- Map to target rule file (pre-created and available for most common foundry targets)
- Run Titan ALX migration with automatic PCells creation and recreate original layout hierarchy
- Stream out migrated design to GDSII or other layout database

Layout Reuse for Engineering Change Orders (ECOs)

- Identify changes in design such as which schematic devices have changes or which devices have been added/deleted
- Implement large changes with Titan AVP or Titan SBR (shape-based router) or favorite layout editor
- Use Titan ALX custom constraints to: open up space in existing layout for adding new devices, create new alignment, matching, symmetry and proximity rules to preserve layout beauty
- Run Titan ALX to create new layout with space added and new structure based on custom constraints
- Do a quick-and-dirty insertion of new devices, and route them by hand with Titan or favorite layout editor
- Re-run Titan ALX to legalize the layout based on the target node DRC rules

Hierarchy and PCell Reuse

- Analyze chip and block congestion and tag critical custom blocks
- For each critical custom block, identify common subcells and tag them
- For each common subcell, analyze design intervals
- Run Titan ALX on critical custom blocks with hierarchy and design intervals
- Run Titan ALX-PCell on critical circuits that need layout PCells for further ECOs

Inputs and Outputs

Input

- Design Migration
 - GDSII Source (existing layout)
 - Layer map from Tech-Source to Tech-Target
 - Source DRM (Design Rule Manual for source technology)
 - Target DRM (Design Rule Manual for target technology)

- Device Resizing
 - Schematic-Source, Schematic-Target
 - OR, device coordinates in GDSII Source, device size in schematic A & B
- PCell Migration
 - PDK-Target, PCell parameter information
- DRC
 - DRC runset for Tech-Target
- LVS
 - Schematic-Source, Schematic-Target
 - LVS runset for Tech-Source and Tech-Target
 - Information about any marker layers used by LVS

Output

- Process migrated GDS

Supported platforms: Linux

MAGMA DESIGN AUTOMATION

Titan™ ALX



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